

PATENT  
5500-91000

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:  
Roger D. Isaac, et al

Serial No. 10/755,734

Filed: January 12, 2004

For: Cache Memory Subsystem  
Including a Fixed Latency  
R/W Pipeline

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Group Art Unit: 21863

Examiner: Unknown

Atty. Dkt. No. 5500-91000

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below:

B. Noel Kivlin  
Registered Representative

6-26-07  
Date

Signature

**NOTICE OF CHANGE OF FEE ADDRESS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

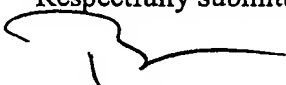
Sir:

Applicant respectfully requests the Commissioner to change the correspondence address for Maintenance Fees with regard to the above identified patent application. The Fee Address is:

AMD – Customer No. 31266

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Respectfully submitted,

  
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